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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED

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Technology Center 2100

Application Number: 10/534,164
Filing Date: May 05, 2005
Appellant(s): MUTH, MATTHIAS

Robert J. Crawford (Reg. No. 32,122)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/14/2007 appealing from the Office action mailed 3/13/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2003/0058894	Feuerstraeter et al.	3-2003
6,674,681	Ishikuri	1-2004
6,292,045	Bongiorno et al.	9-2001
5,778,002	Werle	7-1998

"Electrical Engineering Glossary Definition for V_{cc}", Maxim IC, <http://www.maxim-ic.com/glossary/index.cfm/Ac/V/ID/943/Tm/VEE/In/en>, page 1.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuerstraeter et al. ("Feuerstraeter") (U.S. Patent Application Publication No. 2003/0058894), Applicant's Admitted Prior Art (hereinafter "AAPA"), and Ishikuri (U.S. Patent No. 6,674,681).

Regarding Claim 1, AAPA teaches that to enable synchronization between two communicating devices using a LIN protocol, the receiving device would need to be capable of recognizing certain symbols that differ from those employed by a standard interface (AAPA, Page 1, lines 9-16).

AAPA does not expressly teach an integrated circuit having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset, and a monitoring function, an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte, and a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

In the same field of endeavor (e.g. detection of data transfer rates in a bus system), Feuerstraeter teaches an integrated circuit having

A system base chip (Feuerstraeter, Figure 3, item 340) that has basic functions for a transmitting and/or receiving system for a data bus, namely at least a system voltage supply (Feuerstraeter, Figure 5, see V_{cc} pin located in each of serializer 504 and deserializer 505) and a monitoring function (Feuerstraeter, Figure 7, item 700),

An interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte (Feuerstraeter, Figure 4, item 420, Page 4, paragraphs 0044 and 0047),

A serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit (Feuerstraeter, Figure 3, items 350/360, Page 3, paragraph 0037).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Feuerstraeter's teachings of detection of

data transfer rates in a bus system with the teachings of AAPA, for the purpose of automatically detecting a data transfer rate such that one or more devices may communicate with each other when otherwise the devices would not (see Feuerstraeter, Page 1, paragraph 0011). It also would have been obvious to combine for the purpose of being able to more efficiently communicate with a device of a different protocol by automatically detecting and adjusting for the various differences in the two protocols (i.e., by synchronizing the incoming data by detecting the incoming bit rate, converting between serial and parallel protocols, etc.).

Also in the same field of endeavor (e.g. transmitting and receiving data in an integrated circuit), Ishikuri teaches an integrated circuit having a system voltage supply (Ishikuri, Figure 1, item 1, Column 5, lines 43-56; i.e., see voltage supply entering top of op amp comparator 6), and

A system reset (Ishikuri, Column 5, lines 57-60).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Ishikuri's teachings of transmitting and receiving data in an integrated circuit with the teachings of AAPA, for the purpose of preventing erroneous operations due to runaway of a system (see Ishikuri, Column 5, lines 6-8).

Regarding Claim 6, AAPA teaches the use of an SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface (AAPA, Page 1, lines 13-17).

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuerstraeter, AAPA, and Ishikuri as applied to claim 1 above (hereinafter "FAI"), and further in view of Bongiorno et al. ("Bongiorno") (U.S. Patent No. 6,292,045).

Regarding Claim 2, FAI teaches an oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection (Feuerstraeter, Figure 3, items 480/490, Page 4, paragraph 0044).

FAI does not expressly teach wherein the oscillator is an R/C oscillator.

In the same field of endeavor (e.g. electrical circuits which use clock sources), Bongiorno teaches the use of an R/C oscillator (Bongiorno, Column 1, lines 16-21).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Bongiorno's teachings of electrical circuits which use clock sources with the teachings of FAI, for the purpose of providing an RC oscillator which has the ability to generate high frequency oscillations having a stable frequency characteristic.

Regarding Claim 3, Bongiorno teaches wherein the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor (Bongiorno, Column 1, lines 16-21).

The motivation that was used in the combination of Claim 2, super, applies equally as well to Claim 3.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over FAI, and further in view of Werle (U.S. Patent No. 5,778,002).

Regarding Claims 4 and 5, FAI does not expressly teach wherein the interface circuit may also pass on complete messages and perform buffer-storage of data received or to be transmitted.

In the same field of endeavor (e.g. multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation), Werle teaches wherein an interface circuit may pass on complete messages by performing buffer-storage of data received or to be transmitted (Werle, Figure 1, item 14, Column 3, lines 13-27).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Werle's teachings of multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation with the teachings of FAI, for the purpose of reducing latency of the system if the incoming data rate is slower than that which can be processed.

(10) Response to Argument

Appellant's arguments filed 8/14/2007 have been fully considered but they are not persuasive.

With regards to Claim 1, Appellant argues that "[t]here is no reason to combine the elements in the manner suggested by the Examiner", "[t]he Examiner has relied upon improper hindsight reconstruction", and "[t]he asserted combination of references would defeat the purpose of the primary reference." The examiner disagrees. Contrary

to Appellant's argument, the combination of the references as combined in the Final Office Action is proper. The motivation to combine Feuerstraeter with AAPA would be for the purpose of automatically detecting a data transfer rate such that one or more devices (with differing protocols) may communicate with each other when otherwise the devices would not. Appellant admits that it is known in the art that in order for two devices of differing protocols to be able to communicate with each other, a specially adapted interface or external microcontroller is required in order to enable proper communication (AAPA, paragraph 0004). Accordingly, it is clear that such communications could not occur without some form of protocol adaptation being present. Feuerstraeter teaches that protocol adaptation is known in the art (Feuerstraeter, paragraph 0033). The teachings of Feuerstraeter as described above would eliminate the need for a dedicated external microcontroller to be used to convert (i.e., adapt) between protocols. This would result in less cost to implement the system. Therefore, it can be seen that the motivation used in the Final Office Action was proper. Further, it would have also been obvious to combine the Feuerstraeter reference with AAPA for the purpose of being able to more efficiently communicate with a device of a different protocol by automatically detecting and adjusting for the various differences in the two protocols (e.g., by synchronizing the incoming data by detecting the incoming bit rate, converting between serial and parallel protocols, etc.). In response to Appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it

takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The Supreme Court has held that "a patent for a combination which only unites old elements with no change in their respective functions...obviously withdraws what is already known into the field of its monopoly and diminishes resources available to skillful men...The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 2007 U.S. LEXIS 4745, (U.S. 2007). When a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious. *Sakraida v. AG Pro, Inc.*, 425 U.S. 273 (1976). It can be seen that the operation of the various components, as taught by Feuerstraeter (e.g., a bit rate detector and a serial/parallel converter), with each other in order to detect and to communicate with incoming data of a differing protocol was known. The AAPA teaches the LIN protocol was known. Therefore, since the components disclosed in Feuerstraeter are not limited to the protocols in Feuerstraeter, implementing the LIN protocol as taught by AAPA with Feuerstraeter would have yielded an expected and predictable result. Accordingly, the combination is proper.

Therefore, Appellant's arguments are not persuasive.

Also with regards to Claim 1, Appellant argues that "the cited portions of the Ishikuri reference also do not correspond to the claim limitations directed to the system voltage supply and the system reset." The examiner disagrees. Contrary to Appellant's argument, the integrated circuit 100 of Ishikuri is clearly receiving a system voltage supply, see Figure 1. Within Figure 1, item 1, it can be seen that a voltage source is connected and providing power to the op amp comparator 6. Furthermore, in the instant Appeal Brief, Appellant admits that such a power supply voltage is received in the POC circuit 1 (see Page 7, lines 17-18 under Section (d) in Appeal Brief). Finally, the claimed "system reset" is clearly taught by Ishikuri, see Column 5, lines 57-60 ("POC circuit 1 may be provided to conduct a system reset when a power supply of semiconductor integrated circuit 100 drops below a voltage level..."). Accordingly, it can be seen that Ishikuri does in fact teach the claimed "system voltage supply" and "system reset". In addition, the Feuerstraeter reference also teaches a "system voltage supply", see Figure 5. In each of the serializer 504 and deserializer 505, a V_{CC} pin can be seen located in each circuit. Accordingly, since the circuit symbol V_{CC} is known to correspond to a system voltage supply (see attached "Electrical Engineering Glossary Definition for V_{CC}"), the Feuerstraeter reference also teaches the claimed "system voltage supply".

Therefore, Appellant's arguments are not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be ~~sustained~~.

Respectfully submitted,

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